Analysis and Optimization of CMOS Switched-Capacitor Converters

Visvesh S. Sathe
Department of Electrical Engineering,
University of Washington
Seattle, Washington
Email: sathe@uw.edu

Jae-sun Seo
School of ECEE,
Arizona State University,
Tempe, AZ
Email: jaesun.seo@asu.edu

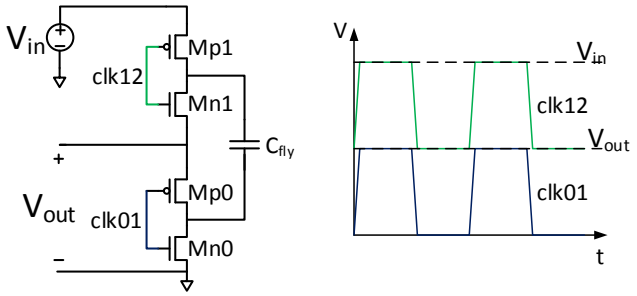
***Abstract*—Energy-efficiency continues to limit peak computational performance in digital systems. To drive continued energy-improvements, designers of modern digital systems are relying on multiple, smaller voltage domains for enhanced voltage-scaling. Switched-capacitor (SC) voltage converters are a promising alternative to traditional switched-inductor regulators due to their suitability for efficient, fully-integrated regulation of finer voltage domains. However, several important problems regarding the analysis and optimization of SC converter design remain unaddressed. This paper develops a comprehensive analysis of SC converter output resistance to establish the optimal switching frequency and switch resistance for maximum converter efficiency. The proposed analysis is validated through simulation experiments conducted using an industrial 65nm CMOS technology.**

I. Introduction

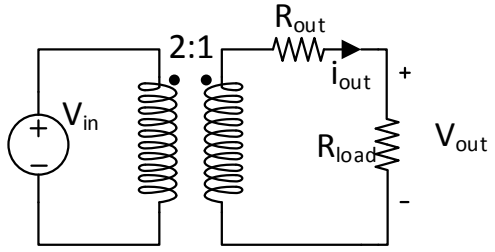
Energy efficiency is a key limiter to continued growth in compute performance [1]. To drive continued energy-efficiency improvements, designers are relying on integrated voltage regulators [2]–[7] to power increasingly smaller domains for finer-grain voltage control and faster supply transitions. This trend is expected to continue – Future Systems-on-Chip (SoCs) are expected to have hundreds of cores [8], each with its own voltage domain.

Supporting a large number of voltage domains poses substantial challenges for package design and device form factor. Efficient integrated voltage conversion and regulation therefore, is the only viable alternative to enabling energy-efficiency through a large number of voltage domains. Using switched capacitors for on-chip voltage regulation has received much interest in recent years [4]–[7], [9]–[12]. For fully-integrated implementations, on-chip capacitors offer a higher quality-factor and energy density [13] compared to switching integrated inductors in existing standard CMOS technologies. Efficient implementations of integrated voltage converters based on switched capacitors have been also demonstrated [4]–[7], [9]. Another promising use for SC converters is in ultra-low power and energy-harvesting systems, particularly for applications that are constrained in total volume. 1:2 and 2:1 converter topologies are overwhelmingly popular [6], [10]–[12] with additional conversion ratios developed by combining individual 1:2 or 2:1 stages [10], [11].

An analytical model for the SC converter is essential for both voltage conversion and regulation. In both applications, the desired output resistance is achieved by modulation of the switching frequency and width [7], [14]. An analysis of optimal switching frequency is offered in [15], but it relies on approximate converter output resistance models that do not accurately reflect the actual operating condition of the converter. Precise expressions for output resistance, and its dependence on switch resistance and switching frequency will enable a better understanding of optimal switching frequency and switch width configurations for efficient SC implementation.



(a) Simplified schematic of a basic 2:1 step-down SC converter. Alternating conduction phases of PMOS and NMOS switches enable the transfer of charge from the supply at V_{in} to the output at $V_{in}/2$.



(b) Simplified 2:1 switched-capacitor converter model.

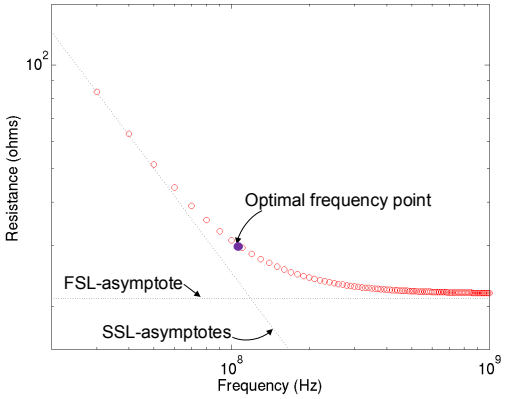
Fig. 1. Simplified 2:1 SC converter model and schematic.

Figure 1 illustrates a simplified schematic, and an electrical model of a 2:1 SC converter. By continuously alternating the connections of the flying capacitor C_{fly} using switches, current is efficiently delivered to the output load at half the voltage. Two key attributes of the converter are its output resistance R_0, and the power dissipation within the converter while driving a load. The converter losses can be written as the sum of P_{sw},

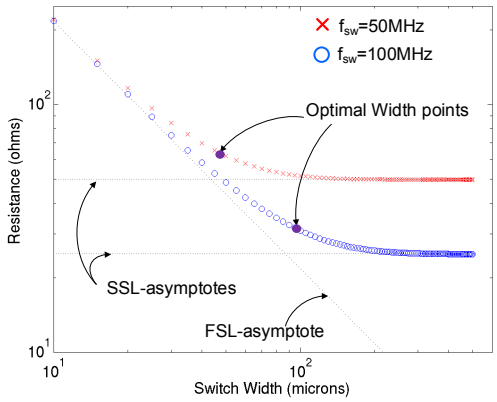
its switching losses and P_{con}, its conduction losses:

$$P_{tot} = P_{sw}(C_{sw}, V_{out}, f_{sw}) + P_{con} \quad (1)$$

where C_{sw} is the switching capacitance associated with driving the switches, V is the voltage swing of the switch gate terminals, and f_{sw} is the converter switching frequency. Typical applications of SC involve design with a target R_0. In such a situation, conduction losses are fixed, and minimizing P_{tot} is equivalent to P_{sw} minimization.



(a) Simulation results of SC converter output resistance vs. switching frequency for a given switch width. The optimal switching frequency yielding maximum efficiency for any given switch width lies between the SSL and FSL regions.



(b) Simulation results of SC converter output resistance vs. switch width at 50MHz and 100MHz switching frequency. The optimal switch width yielding maximum efficiency for any given frequency lies between SSL and FSL regions.

Fig. 2. Simulated 2:1 SC converter R_0 vs. switching frequency and switch width.

Prevalent resistance models for SC converters are applicable to the the Slow Switching Limit (SSL), and the Fast Switching Limit (FSL). During the SSL, the converter is assumed to be switching slowly enough for C_{fly} to completely charge (discharge) when connected to V_{in} (V_{out}). Under the FSL regime, the switching frequency is high enough for the voltage change across the capacitor to be small, and the current flow through the switches to be essentially constant. The output resistance of a general SC converter under the FSL and SSL regimes is well understood [16] and in the case of a 2:1 SC converter, reduces to:

$$\begin{aligned} R_{SSL} &= \frac{1}{4f_{sw}C} \\ R_{FSL} &= 2R_{sw}, \end{aligned} \quad (2)$$

where R_{sw} is the resistance of each switch used in the converter. Observe that R_{SSL} does not depend on switch resistance, while R_{FSL} is independent of switching frequency. Figure 2 shows simulation results of the output resistance of a 2:1 converter as a function of frequency and switch width. As seen from the Figure, the two resistance metrics are really only asymptotes. More importantly, the region of interest for minimum converter losses for a given output resistance lies between the two limits.

Recent work has established closed-form expressions for 1:2 and 2:1 SC converter output resistance [17], [18]. However, several important aspects of SC converters require closer examination. Understanding optimal switching frequency and switch width that will yield maximum efficiency will enable not only efficient converters, but also provide insight into effective compensation techniques for regulator applications. power-optimal design of SC voltage converters. The scope of this work will cover the design of 2:1 and 1:2 converter circuits, which are overwhelmingly used in actual implementations due to their efficiency, and their ability to provide other conversion ratios [10], [11]. The contributions of this paper are as follows: (1) We build upon existing work in SC converter analysis [17], [18] to develop a closed form expression for switched-capacitor output resistance. (2) We identify the criterion for optimal switch width allocation and f_{sw} to provide a target output resistance with maximum energy efficiency. (3) Using our optimization results, we propose a control law for the simultaneous scaling of the switching frequency and switch width. We validate our analysis by comparison with simulations of SC-converter designs performed in an industrial 65-nm CMOS technology and present our results.

The remainder of this paper is organized as follows: Section II presents the analysis leading to a closed-form resistance expression for a 2:1 and 1:2 SC converter. Section III presents analysis on the energy-optimal configuration of SC converters, and a discussion of a control law to maximize R_0 constrained efficiency in SC regulators. Comparisons of the analysis with simulation experiments in an industrial 65nm CMOS process are presented in Section IV.

II. Switched Capacitor Converter Analysis

In this section, we will build upon the closed-form expressions for 1:2 and 2:1 SC converters to enable the formulation of the problem of power-optimization in the converter.

The analysis in the current section, and upon which subsequent optimization criterion and sizing guidelines are derived, makes the following assumptions:

A1 The generation of the clock signals for the SC converter switches can be performed using a variety of different techniques [6], [14], [15]. To maintain generality, the ensuing analysis assumes that the switching power dissipation

in the converter can be written as:

$$P_{sw} = P_0 + k_{drive} C_{sw} V^2 f_{sw} \ , \tag{3}$$

Where P_0 is the power overhead in implementing the switch drivers, C_{sw} is the combined switching capacitance in the switches, and k_{drive} is the constant of proportionality accounting for the pre-drivers.

A2 The total power dissipation of the converter is assumed to be dominated by switching losses and conduction losses. Losses due to device leakage in the converters are ignored.

A3 Inclusion of the bottom-plate capacitance requires the use of numerical techniques for optimization. For simplicity, bottom-plate capacitance is ignored in this analysis.

As a result of the last two simplifying assumptions, the proposed analysis is suitable for medium and high-power SC converter applications. Analysis of low-power converter applications requires incorporation of leakage and bottom-place capacitance effects into Equation (3), which can be solved using numerical techniques.

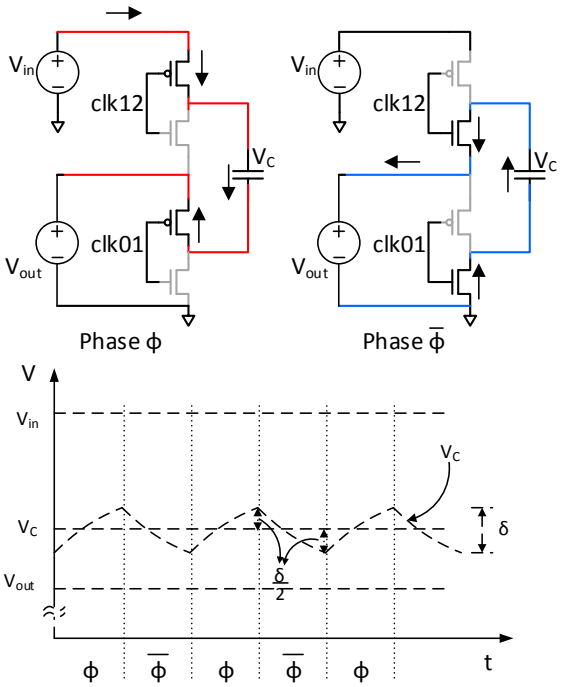


Fig. 3. Steady-state voltage across C_{fly} from Figure 1. C_{fly} does not discharge completely, and the magnitude of current flow is not constant during the entire conduction phase of each switch.

Figure 3 illustrates the circuit used to determine the output resistance of a SC converter. The analysis proceeds with the placement of a voltage source V_{out} at the output of the converter in order to determine the R_0 based on the the resulting output current flow. In such a configuration:

$$R_0 = \frac{\frac{V_{in}}{2} - V_{out}}{I_{load}} \ . \tag{4}$$

As depicted in Figure 3, under steady-state conditions, the voltage transition experienced by C_{fly} (denoted as δ) during phases ϕ and $\overline{\phi}$ is equal. During ϕ, with C_{fly} connected in series with the output load and the input supply, the voltage increase can be written as:

$$\delta = (V_{in} - (V_C - \frac{\delta}{2}) - V_{out})(1 - e^{\frac{-t_r}{2\tau_r}}) \ , \tag{5}$$

where t_r is the duration of time for which the circuit stays in phase ϕ, and $2\tau_r$ is the RC time constant associated with the two PMOS devices in series with C_{fly}. Similarly, the decrease in the voltage across C_{fly} during $\overline{\phi}$, when C_{fly} is connected in parallel with the output load, can be written as:

$$\delta = (V_C + \frac{\delta}{2} - V_{out})(1 - e^{\frac{-t_f}{2\tau_f}}) \ , \tag{6}$$

where t_f is the duration of time for which the circuit stays in phase $\overline{\phi}$, and $2\tau_f$ is the RC time constant associated with the NMOS two devices in series with C_{fly}. Simplifying Equation 5 yields

$$\begin{aligned} V_{in} - V_C - V_{out} &= \frac{\delta}{1 - e^{\frac{-t_r}{2\tau_r}}} - \frac{\delta}{2} \\ &= \frac{\delta}{2}(\frac{1 + e^{\frac{-t_r}{2\tau_r}}}{1 - e^{\frac{-t_r}{2\tau_r}}}), \end{aligned} \tag{7}$$

Similarly, simplifying Equation (6) yields

$$\begin{aligned} V_C - V_{out} &= \frac{\delta}{1 - e^{\frac{-t_f}{2\tau_f}}} - \delta \\ &= \frac{\delta}{2}(\frac{1 + e^{\frac{-t_f}{2\tau_f}}}{1 - e^{\frac{-t_f}{2\tau_f}}}) \end{aligned} \tag{8}$$

Adding Equations (5) and (6) to eliminate V_C and dividing by 2 gives:

$$\begin{aligned} \frac{V_{in}}{2} - V_{out} &= \frac{\delta}{4}(\frac{1 + e^{\frac{-t_r}{2\tau_r}}}{1 - e^{\frac{-t_r}{2\tau_r}}} + \frac{1 + e^{\frac{-t_f}{2\tau_f}}}{1 - e^{\frac{-t_f}{2\tau_f}}}) \\ &= \frac{\delta}{4}(coth\frac{t_r}{4\tau_r} + coth\frac{t_f}{4\tau_f}). \end{aligned} \tag{9}$$

The charge delivered by a 2:1 converter over a single cycle is $2C_{fly}\delta$. Combining equations 4 and 9, we arrive at an expression for the output resistance:

$$\begin{aligned} R_0 &= (\frac{V_{in}}{2} - V_{out})\frac{1}{I_{load}} \\ &= (\frac{V_{in}}{2} - V_{out})\frac{1}{2C_{fly}\delta f_{sw}} \\ &= \frac{1}{8C_{fly}f_{sw}}(coth\frac{t_r}{4\tau_r} + coth\frac{t_f}{4\tau_f}) \end{aligned} \tag{10}$$

Equation (10) specifies the output resistance of the SC converter as a function of t_r, t_f, τ_r, τ_f, C_{fly} and f. The optimal duty cycle can be determined by setting $\partial R/\partial D = 0$ where $T = 1/f_{sw}$, and DT is the duration of phase ϕ.

$$\begin{aligned} R_0 &= \frac{1}{8C_{fly}f_{sw}}(coth\frac{DT}{4\tau_r} + coth\frac{(1-D)T}{4\tau_f}) \\ \frac{\partial R_0}{\partial D} &= \frac{T}{32C_{fly}f}(-\frac{1}{\tau_r}cosech^2\frac{DT}{4\tau_r} + \frac{1}{\tau_r}cosech^2\frac{(1-D)T}{4\tau_f}) = 0, \end{aligned} \tag{11}$$

For the case when $\tau_r = \tau_f$, and observing that cosech(x) is injective over the range $(0, \infty)$ yields an expected result of $D = 0.5$. For the remainder of this analysis we assume $\tau_r = \tau_f = \tau$, yielding:

$$R_0 = \frac{1}{4C_{fly}f}coth\frac{T}{8\tau}. \tag{12}$$

Equation (12) can be shown to be consistent with the well-

known equations of output resistance at the SSL and FSL limits (Equation (2)). Re-writing Equation (12):

$$\begin{aligned} R_0 &= \frac{1}{4C_{fly}f}\frac{1+e^{\frac{-T}{4\tau_r}}}{1-e^{\frac{-T}{4\tau_r}}} \\ &= \frac{1}{4C_{fly}f}\ as\ T \rightarrow \infty \end{aligned} \tag{13}$$

To verify the expression as $T \rightarrow 0$, Equation (14) is first re-written as:

$$\begin{aligned} R_0 &= \frac{1}{4C_{fly}f}\frac{1+(1-\frac{-T}{4\tau_r}+...)}{1-(1+\frac{-T}{4\tau_r}+...)} \\ &= \frac{1}{4C_{fly}f}\frac{2}{\frac{T}{4\tau_r}} \\ &= \frac{1}{4C_{fly}f}\frac{8R_{sw}C_{fly}}{T} \\ &= 2R_{sw}. \end{aligned} \tag{14}$$

Note that in the event that $\tau_r = \tau_f$, it can also be shown that $V_C = {}^{V_{in}}/_2$. A similar analysis results in the following expression for a 1:2 step-up converter:

$$R_0 = \frac{1}{C_{fly}f}coth\frac{T}{8\tau}. \tag{15}$$

In the next section, we will develop our analysis to minimize power dissipation within a 2:1 SC converter while maintaining a target output resistance.

III. SC Converter Optimization

A. Deriving f_{sw} for maximum energy

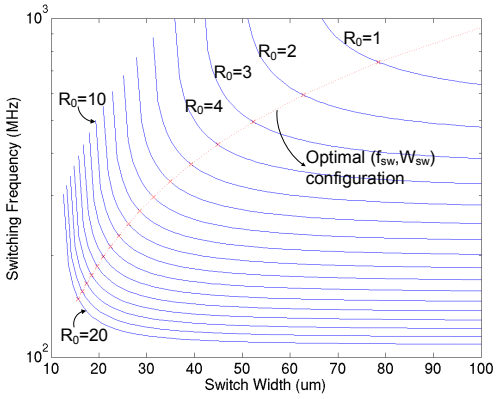


Fig. 4. Switch width, W_{sw} and switching frequency, f_{sw} can be traded-off to achieve a target resistance. Each output resistance has an (f^*_{sw},W^*_{sw}) assignment corresponding to maximum converter efficiency.

In this section, we examine the optimal values of f_{sw} and W_{sw} that maximize converter efficiency while meeting target output resistance, R_0 . When used for voltage regulation applications [7], an R_0 constraint ensures a controlled drop-out against a peak current load, enabling sufficient headroom for the downstream voltage regulator to ensure a steady output voltage. When used in conjunction with a feedback loop to directly regulate a supply voltage, a compensator modulates switching frequency and switch width so as to maintain a target voltage at the regulator output. As shown in Equation (12), and illustrated in Figure 4, a variety of possible W_{sw} and f_{sw} combinations exist, all providing the same R_0. The problem of maximizing converter efficiency while maintaining an output resistance of R_0 can be stated as:

$$\begin{aligned} &minimize && P_{tot} = kC_{sw}V^2f_{sw} + I^2_{load}R_0 \\ &s.t. && \frac{1}{4C_{fly}f}coth\frac{T}{8\tau} = R_0, \end{aligned} \tag{16}$$

This section will derive the conditions on f_{sw} and W_{sw} to achieve maximum energy efficiency. Although a 2:1 converter will be used as an example, the results are similarly applicable to a 1:2 converter design.

First, we observe that minimizing P_{tot} is equivalent to minimizing the switching losses in the regulator since both I_{load} and R_0 are not optimization variables. Focusing on the switching power of the converter, the dissipation P_{sw} is re-written as:

$$\begin{aligned} P_{sw} &= k_{drive}C_{sw}V^2f_{sw} \\ &= \frac{kC_{sw}R_{sw}C_{fly}V^2f_{sw}}{R_{sw}C_{fly}} \\ &= \frac{k\tau_{sw}C_{fly}V^2f_{sw}}{\tau}, \end{aligned} \tag{17}$$

where τ_{sw}, dependent on input supply voltage and process technology, is a constant for our analysis. The constrained optimization problem can be written as an unconstrained single-variable minimization problem by writing τ in terms of R_0 in Equation (12) and substituting for τ in Equation (18):

$$P_{sw} = 8k\tau_{sw}C_{fly}V^2f^2_{sw}coth^{-1}(4R_0f_{sw}C_{fly}), \tag{18}$$

The switching frequency f^*_{sw} corresponding to maximum converter efficiency therefore can be obtained by setting ${}^{\partial P_{sw}}/_{\partial f_{sw}} = 0$. The resulting expression is:

$$\begin{aligned} 2coth^{-1}(4R_0C_{fly}f_{sw}) &= \frac{4R_0C_{fly}f_{sw}}{16R^2_0C^2_{fly}f^2_{sw}-1} \\ 2coth^{-1}\alpha &= \frac{\alpha}{\alpha^2-1}, \end{aligned} \tag{19}$$

where $\alpha = 4R_0C_{fly}f_{sw}$. A numerical analysis yields $\alpha = 1.26$ as a solution to Equation (19). Consequently, the value of the optimal switching frequency, f^*_{sw} is found to be

$$f^*_{sw} = \frac{1.26}{4R_0C_{fly}} \tag{20}$$

The similarity of the the result described in Equation (20) to the output resistance at the SSL in Equation (2) is both remarkable and useful. Given target resistance R_0, the optimal switching frequency f^*_{sw} is obtained by scaling the SSL-based switching frequency approximation by a factor of 1.26.

B. Deriving W_{sw} for maximum energy

Given f^*_{sw} , W^*_{sw} can be readily obtained by substituting f^*_{sw} into Equation (12), and recalling the definition of α,

$$\begin{aligned} \tau &= \frac{1}{8f^*_{sw}coth^{-1}(4R_0f^*_{sw}C_{fly})} \\ &= \frac{1}{8f^*_{sw}coth^{-1}\alpha} \end{aligned} \tag{21}$$

Since $\alpha = 1.26$ for maximum efficiency, and f^*_{sw} has been obtained from Equation (20), substitution into (21) yields another straightforward result for the optimal switch resistance $R^*_{sw} \equiv {}^{k_{sw}}/_{W^*_{sw}}$.

$$\begin{aligned} R^*_{sw} &= 0.37R_0 \\ W^*_{sw} &= \frac{k_{sw}}{0.37R_0}. \end{aligned} \tag{22}$$

Similar to Equation (20), (22) yields a surprisingly simple and useful result. To maximize converter efficiency, the size of each switch in the converter should be chosen so that its on-resistance is a fixed fraction of the target resistance R_0, regardless of operating voltage, value of C_{fly} and even f_{sw}. Note that although the analysis can be used to show that the optimal configuration corresponds to neither FSL or SSL (illustrated in Figure 2), the value for f^*_{sw} and W^*_{sw} can be determined by scaling the results obtained from Equation (2).

C. Applications to Regulation

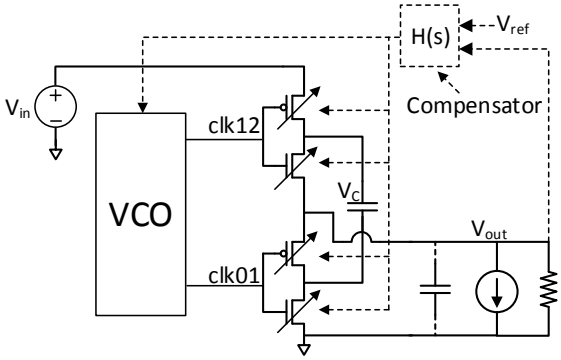


Fig. 5. Example of a SC voltage converter used for voltage regulation. As the load current fluctuates, a compensator scales the switch width, and modulates the Voltage-Controlled Oscillator (VCO) frequency to maintain a target output voltage.

Figure 5 shows an example implementation of a SC converter-based regulator. The use of simultaneous modulation of both frequency and switch width has been adopted in the past [6], [7], but an efficient control law for the modulation of the converter output resistance has not been derived to date. Drawing from Equations (20) and (22), which specify the optimal values of f_{sw} and W_{sw} for efficient converter operation, the relationship between f_{sw} and W_{sw} is observed to be

$$f^*_{sw} = \frac{1}{4R_0C_{fly}} = \frac{0.46}{4k_{sw}C_{fly}}W_{sw}, \quad (23)$$

Indicating a specific linear relationship that should be maintained between VCO frequency to the applied switch width for efficient operation.

IV. Model Validation

To validate the accuracy of our analysis, we compared simulation results of a 2:1 switched capacitor implementation with $V_{in} = 1.2V$, $C_{fly} = 1nF$ in a 65nm industrial CMOS process. For a range of possible target resistances, R_0, simulations were performed to identify the f_{sw}, W_{sw} combinations that yielded the highest power efficiency in the converter.

Figure 6 compares the simulated SC converter output resistance over a range of values of f_{sw}. The proposed model agrees well with simulation results. In particular, unlike the SSL and FSL limits, the proposed model yields improved accuracy in the intervening region which is relevant for optimal converter operation. Figure 7 illustrates the relationship between R_0

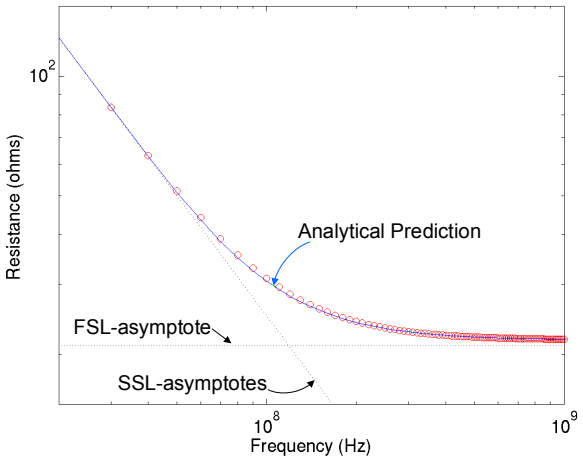


Fig. 6. Simulation results of the output resistance of a 2:1 converter versus f_{sw}. R_0, versus switching frequency f_{sw}. Analytical predictions of this relationship based on Equation (12) are super-imposed

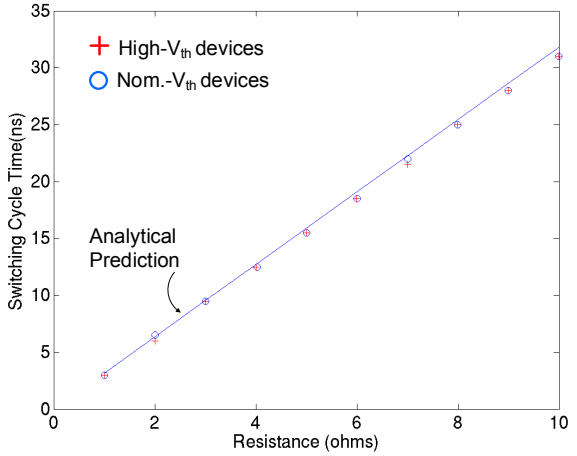


Fig. 7. Target resistance R_0, versus optimal switching frequency f^*_{sw} for maximum converter power efficiency. Analytical predictions of the relation based on Equation (20) are super-imposed.

and f^*_{sw} using both using nominal-V_{th} and high-V_{th} devices. As seen from the figure, analytical predictions based on the proposed model agree well with simulated points. As expected from Equation (20), and confirmed by the simulation, the choice of threshold voltage, or other parameters affecting the switch resistance do not impact the choice of f^*_{sw}.

Figure 8 shows the relationship between R_0 and $1/W^*_{sw}$ using both using nominal-V_{th} and high-V_{th} devices. The analytical model accurately matches simulation results. Also shown on the plot are estimates of required W_{sw} based on FSL operation. As discussed in Section II, the $W^*_{sw} - R_0$ curve can be obtained by scaling up the estimates obtained from FSL assumptions, resulting in a gradient offset.

Figure 9 shows simulation results of minimum achievable SC converter power versus target R_0 for two designs using nominal-V_{th} and high-V_{th} respectively. In addition to the sim-

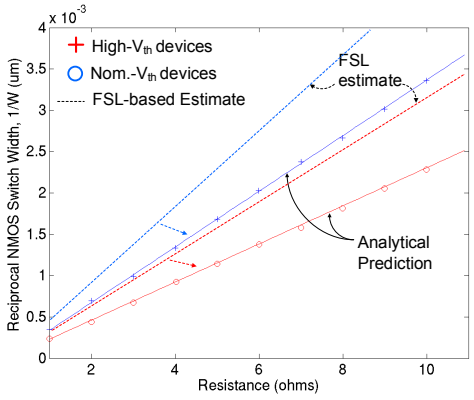


Fig. 8. Target resistance R_0, versus optimal switch width W^*_{sw} for maximum converter power efficiency at $f_{sw} = 100MHz$ and $200MHz$. Analytical predictions of the relation based on Equation (22) are super-imposed.

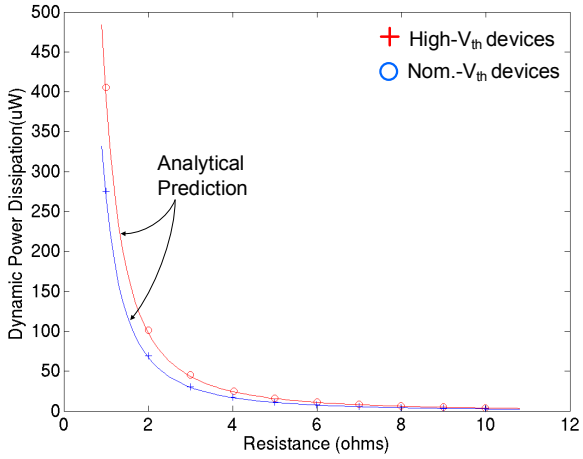
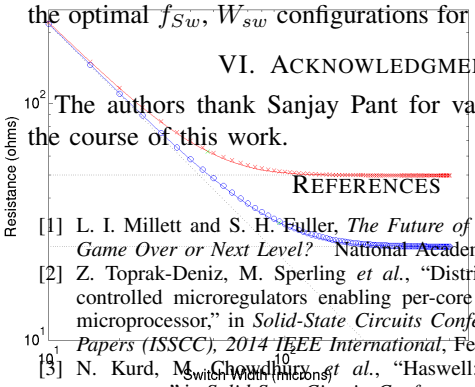


Fig. 9. Target resistance R_0, versus optimal switch width W^*_{sw} for maximum converter power efficiency. Analytical predictions of the derived based on Equation (18) are super-imposed.

ulated dynamic power, the predicted power dissipation based on Equation (18) is also shown .

V. Conclusion

In this paper, we developed a general closed-form expression of output resistance in 1:2 and 2:1 converters to obtain output-resistance constrained power-optimal assignments for the converter switching frequency and switch width. Simulation experiments carried out in an industrial 65nm process technology agree well with our proposed analysis. We find that although the optimal switching frequency and switch widths correspond to converter operation that is neither in the Fast Switching Limit nor the Slow Switching Limit, they can be obtained by simply scaling the values of frequency and switch width predicted by the simple equations that govern these operating regimes. Furthermore, the analysis provides a control law to optimally, simultaneously scale frequency and switch width for SC converters and regulators. Future work involves determining the optimal criterion for general conversion ratios, determining the optimal f_{Sw}, W_{sw} configurations for non-unity beta ratios.



VI. Acknowledgments

The authors thank Sanjay Pant for valuable discussions in the course of this work.

References

[1] L. I. Millett and S. H. Fuller, *The Future of Computing Performance:: Game Over or Next Level?* National Academies Press, 2011.

[2] Z. Toprak-Deniz, M. Sperling *et al.*, "Distributed system of digitally controlled microregulators enabling per-core DVFS for the POWER8 microprocessor," in *Solid-State Circuits Conference Digest of Technical Papers (ISSCC), 2014 IEEE International*, Feb 2014, pp. 98–99.

[3] N. Kurd, M. Chowdhury *et al.*, "Haswell: A family of IA 22nm processors," in *Solid-State Circuits Conference Digest of Technical Papers (ISSCC), 2014 IEEE International*. IEEE, 2014, pp. 112–113.

[4] T. Andersen, F. Krismer *et al.*, "A 4.6w/mm2 power density 86% efficiency on-chip switched capacitor DC-DC converter in 32 nm SOI CMOS," in *2013 Twenty-Eighth Annual IEEE Applied Power Electronics Conference and Exposition (APEC)*, Mar. 2013, pp. 692–699.

[5] T. Anderson, F. Krismer *et al.*, "A deep trench capacitor based 2:1 and 3:2 reconfigurable on-chip switched capacitor DC-DC converter in 32 nm SOI CMOS," in *2014 Twenty-Ninth Annual IEEE Applied Power Electronics Conference and Exposition (APEC)*, Mar. 2014, pp. 1448–1455.

[6] W. Jung, S. Oh *et al.*, "23.3 A 3nW fully integrated energy harvester based on self-oscillating switched-capacitor DC-DC converter," in *Solid-State Circuits Conference Digest of Technical Papers (ISSCC), 2014 IEEE International*, Feb 2014, pp. 398–399.

[7] G. Patounakis, Y. Li, and K. L. Shepard, "A fully integrated on-chip DC-DC conversion and power management system," *IEEE Journal of Solid-State Circuits*, vol. 39, no. 3, pp. 443–451, Mar. 2004.

[8] S. Borkar and A. A. Chien, "The future of microprocessors," *Communications of the ACM*, vol. 54, no. 5, pp. 67–77, 2011.

[9] H.-P. Le, M. Seeman *et al.*, "A 32nm fully integrated reconfigurable switched-capacitor DC-DC converter delivering 0.55w/mm2 at 81% efficiency," in *Solid-State Circuits Conference Digest of Technical Papers (ISSCC), 2010 IEEE International*, Feb. 2010, pp. 210–211.

[10] S. Bang, A. Wang *et al.*, "A fully integrated successive-approximation switched-capacitor dc-dc converter with 31mv output voltage resolution," in *Solid-State Circuits Conference Digest of Technical Papers (ISSCC), 2013 IEEE International*, Feb 2013, pp. 370–371.

[11] L. Salem and P. Mercier, "4.6 An 85%-efficiency fully integrated 15-ratio recursive switched-capacitor DC-DC converter with 0.1-to-2.2v output voltage range," in *Solid-State Circuits Conference Digest of Technical Papers (ISSCC), 2014 IEEE International*, Feb. 2014, pp. 88–89.

[12] Y. Ramadass and A. Chandrakasan, "Voltage Scalable Switched Capacitor DC-DC Converter for Ultra-Low-Power On-Chip Applications," in *IEEE Power Electronics Specialists Conference, 2007. PESC 2007*, Jun. 2007, pp. 2353–2359.

[13] M. Seeman, V. Ng *et al.*, "A comparative analysis of Switched-Capacitor and inductor-based DC-DC conversion technologies," in *2010 IEEE 12th Workshop on Control and Modeling for Power Electronics (COMPEL)*, Jun. 2010, pp. 1–7.

[14] H.-P. Le, J. Crossley *et al.*, "A sub-ns response fully integrated battery-connected switched-capacitor voltage regulator delivering 0.19w/mm2 at 73% efficiency," in *Solid-State Circuits Conference Digest of Technical Papers (ISSCC), 2013 IEEE International*, Feb 2013, pp. 372–373.

[15] H.-P. Le, S. Sanders, and E. Alon, "Design Techniques for Fully Integrated Switched-Capacitor DC-DC Converters," *IEEE Journal of Solid-State Circuits*, vol. 46, no. 9, pp. 2120–2131, Sep. 2011.

[16] M. Seeman and S. Sanders, "Analysis and optimization of switched-capacitor dc-dc converters," *Power Electronics, IEEE Transactions on*, vol. 23, no. 2, pp. 841–851, March 2008.

[17] S. Ben-Yaakov and M. Evzelman, "Generic and unified model of Switched Capacitor Converters," in *IEEE Energy Conversion Congress and Exposition, 2009. ECCE 2009*, Sep. 2009, pp. 3501–3508.

[18] J. Henry and J. Kimball, "Practical Performance Analysis of Complex Switched-Capacitor Converters," *IEEE Transactions on Power Electronics*, vol. 26, no. 1, pp. 127–136, Jan. 2011.