Visvesh S. Sathe

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CURRENT RESEARCH INTERESTS

Self-optimizing VLSI Systems

Energy-Efficient VLSI Circuits and Architectures **Next generation clocking – Circuits and architectures**

VLSI for Machine Learning **Integrated switching regulators**

EDUCATION

2007 Doctor of Philosophy in Electrical Engineering, **University of Michigan, Ann Arbor**
Thesis: Hybrid Resonant-Clocked Digital Design. Advisor: Marios C. Papaefthymiou.

2004 Master of Science in Electrical Engineering, **University of Michigan, Ann Arbor**

2001 Bachelor of Technology in Electrical Engineering, **Indian Institute of Technology**, Bombay

RESEARCH EXPERIENCE

- Adaptive circuit design and power management
- Low-power VLSI circuits
- Power supply analysis and droop mitigation techniques
- High performance digital design
- Charge-recycling for energy-efficient digital design
- Switching voltage regulator design
- Integrated resonant clocking
- High performance clocking and frequency synthesis
- Clock synchronization
- Circuit design for accurate voltage and time-measurement

PROFESSIONAL EXPERIENCE

UNIVERSITY OF WASHINGTON, SEATTLE

Assistant Professor **Sep 2013 – present**

ADVANCED MICRO DEVICES, FORT COLLINS, CO

Member of Technical Staff, Low-Power Advanced Development Group **Jun 2011 – Jun2013**

- Technical lead - Resonant Clocking. Solved several open problems which were preventing the viability of resonant clocking, enabling the implementation of the first-ever resonant-clocked commercial microprocessor. Drove concept, design and test of feature in AMDs 32nm Piledriver and 28nm Steamroller processor cores.
- Presently conducting research on Integrated Voltage Regulation circuits and control systems for next-generation microprocessors.
- Subject matter expert in clock design. Devised clock optimization algorithms adopted by product clock teams for low-skew energy-efficient clock design.

Senior Design Engineer, Advanced Power Technology Group **Aug. 2007 – Jun. 2011**

- Devised technique for supply droop mitigation through clock-phase modulation. Proposed technique is currently incorporated into AMD's 28nm processor core.
- Invented energy-efficient switched-capacitor voltage converter circuits for integrated supply regulation.
- Developed novel critical path monitor and sub-picosecond accurate delay measurement technique in 32nm SOI for use in AMD GPUs.
- Devised and implemented novel Digital Frequency Synthesis architecture in 32nm SOI for single cycle frequency modulation. Proposed technique allows fine-grain core performance modulation without associated relock-time.
- Led clock-power optimization for the Bulldozer family of cores.
- Designed supply noise measurement circuits in 32nm SOI.

THE UNIVERSITY OF MICHICAN, ANN ARBOR, MI

Graduate Student Research Assistant **Sep. 2001 – May 2007**

- Devised and implemented the first GHz-class fully-integrated resonant-clocked datapaths in 0.13µm CMOS.
- Developed linear programming based static-timing framework for resonant-clocked datapaths.
- Invented charge-recovery logic operating with a sub-threshold supply voltage capable of GHz-class frequencies.
- Developed and implemented the first GHz charge recovery-logic and test-chip in 0.13µm CMOS.

IBM T. J. WATSON RESEARCH LAB, YORKTOWN HEIGHTS, NY

Summer Co-op I **May. 2003 - Aug 2003**

- Devised a novel technique to enable efficient data communication across clock domains with rationally related frequencies using a generalized DLL architecture.

Summer Co-op II **Jun. 2004 - Aug 2004**

- Physical design of the IBM Eclipse processor in 65nm CMOS.

TEACHING EXPERIENCE

VLSI Design I (EECS 427) : Instructor	**Winter 2007**
Special Topics in Electronic Circuit Design (EE538) : Instructor	**Fall 2013**
VLSI Design I (EE 476) : Instructor	**Fall 2014**

PUBLICATIONS

A. Journal Articles

1. **V. S. Sathe**, S. Arekapudi, A. Ishii, C. Ouyang, M. C. Papaefthymiou, S. Naffziger, "Resonant Clock Design for a Power-efficient, High-volume x86-64 Microprocessor", to appear in *IEEE Journal of Solid-State Circuits*, ***Invited paper***, *Special Issue on ISSCC '12,* Jan. 2013.
2. W. S. Ma, J. C. Kao, **V. S. Sathe**, and M. C. Papaefthymiou, "187MHz subthreshold-supply charge-recovery FIR," *IEEE Journal of Solid-State Circuits*, ***Invited paper***, *Special Issue on 2009 Symposium on VLSI Circuits,* vol. 45, no. 4, pp. 793–803, Apr. 2010.
3. **V. S. Sathe**, J. Kao and M. C. Papaefthymiou, "Resonant-clock latch-based design", *IEEE Journal of Solid-State Circuits, **Invited paper**, Special Issue on 2007 Symposium on VLSI Circuits,* vol. 43, no. 4, pp. 864–873, Apr. 2008.
4. **V. S. Sathe**, J.-Y. Chueh, and M. C. Papaefthymiou, "Energy-efficient GHz-class charge-recovery logic," *IEEE Journal of Solid-State Circuits, **Invited paper**, Special Issue on ISSCC '06*, vol. 42, no. 1, pp. 38–47, Jan. 2007.
5. **V. S. Sathe**, M. C. Papaefthymiou, S. V. Kosonocky, and S. Kim, "On-chip synchronous communication between clock domains with quotient frequencies," *Electronics Letters*, vol. 43, no. 9, pp. 497–499, Apr. 2007.

B. Conference Publications

1. **V. S. Sathe**, "Quasi-Resonant Clocking : A Run-time Control Approach for True Voltage-Frequency-Scalability," to appear in *IEEE ISLPED*, La Jolla, 2014.
2. K. Sankaragomathi, W. A. Smith and **V. S Sathe**, "A deterministic-dither-based, all-digital system for on-chip power supply noise measurement", to appear in *IEEE ISLPED,* La Jolla, 2014.
3. **V. S. Sathe**, A. Loke, T. Khan, V. Ross, A. Raman, G. Vandevalk, P. Papadopoulos and N. Provatas, "Inductor Design for Global Resonant Clock Distribution," in *Design Automation Conference*, Austin, 2013.
4. **V. S. Sathe**, S. Arekapudi, A. Ishii, C. Ouyang, M. Papaefthymiou and S. Naffziger, "Resonant clock design for a power-efficient, high-volume x86-64 microprocessor," in *IEEE Int. Solid-State Circuits Conference*, pp. 68-69 San Francisco, CA, Feb. 2012. **An extended version of this paper was invited for publication** in the *IEEE Journal of Solid-State Circuits*, Special Issue on ISSCC '12.
5. H.-P. Le, M. Seeman, S. Sanders, **V. S. Sathe**, S. Naffziger, and E. Alon, "A 32nm fully-integrated reconfigurable switched-capacitor DC-DC converter delivering 0.55W/mm2 at 77% efficiency," *in IEEE*

Int. Solid-State Circuits Conference, pp. 210–211, San Francisco, CA, Feb. 2010.

6. J. C. Kao, W. S. Ma, **V. S. Sathe**, and M. C. Papaefthymiou, "A charge-recovery 600MHz FIR filter with 1.5-cycle latency overhead," in *IEEE European Solid-State Circuits Conference(ESSCIRC)*, pp. 160–163, Athens, Greece, Sep. 2009.
7. M. C. Papaefthymiou, A. Ishii, J. Kao., and **V. S. Sathe**, "A resonant-clock 200MHz ARM926EJ-S™ microcontroller," in *IEEE European Solid-State Circuits Conference(ESSCIRC)*, pp. 356–359, Athens, Greece, Sep. 2009.
8. W. S. Ma, J. C. Kao, **V. S. Sathe**, and M. C. Papaefthymiou, "A 187MHz subthreshold-supply robust FIR filter with charge-recovery logic," *in IEEE Symposium VLSI Circuits*, pp. 202–203, Kyoto, Japan, Jun. 2009. **An extended version of this paper was invited for publication** in the *IEEE Journal of Solid-State Circuits, Special Issue on VLSI Circuits '09*.
9. **V. S. Sathe**, J. C. Kao, and M. C. Papaefthymiou, "RF2: A 1GHz FIR filter with distributed resonant clock generator," *in IEEE Symposium VLSI Circuits*, pp. 44–45, Kyoto, Japan, Jun. 2007. **An extended version of this paper was invited for publication** in the *IEEE Journal of Solid-State Circuits, Special Issue on VLSI Circuits '07*.
10. **V. S. Sathe**, J-Y. Chueh, and M. C. Papaefthymiou, "A 1.1GHz charge-recovery logic," in *IEEE Int. Solid-State Circuits Conference*, pp. 1540–1549, San Francisco, CA, Feb. 2006. **An extended version of this paper was invited for publication** in *the IEEE Journal of Solid-State Circuits, Special Issue on ISSCC'06*.
11. **V. S. Sathe**, J. C. Kao, and M. C. Papaefthymiou, "A 0.8-1.2GHz single-phase resonant-clocked FIR filter with level-sensitive latches," in Proc. *IEEE Custom Integrated Circuits Conference*, pp. 583–586, San Jose, CA, Sep. 2007.
12. J.-Y. Chueh, **V. S. Sathe**, and M. C. Papaefthymiou, "900MHz to 1.2GHz two-phase resonant clock network with programmable driver and loading," in Proc. *IEEE Custom Integrated Circuits Conference(CICC)*, pp. 777–780, San Jose, CA, Sep. 2006.
13. **V. S. Sathe**, C. H. Ziesler, and M. C. Papaefthymiou, "A GHz-class charge-recovery logic," in *Int. Symposium Low-Power Electronic Design(ISPLED)*, pp. 91–94, San Diego, CA, Aug. 2005.
14. **V. S. Sathe**, J-Y. Chueh, J. Kim, C.H. Ziesler, S. Kim, and M. C. Papaefthymiou, "Fast, efficient, recovering and irreversible," in *Conference on Computing Frontiers*, pp. 407–413, Ischia, Italy, May 2005.
15. J-Y. Chueh, **V. S. Sathe** and M. C. Papaefthymiou, "Two-phase resonant clock distribution," *in Int. Symposium VLSI*, pp. 65–70, Tampa, FL, May 2005.
16. **V. S. Sathe**, C. H. Ziesler and M. C. Papaefthymiou, "Boost logic: a high-speed energy-recovery circuit family," in *Int. Symposium VLSI*, pp. 22–27, Tampa, FL, May 2005.
17. **V. S. Sathe**, S. Kim, S. Kosonocky, and M. C. Papaefthymiou, "A synchronous interface for SoCs with multiple clock domains," in *SOC Conference*, pp. 173–174, Newport Beach, CA, Sep. 2004.
18. C. H. Ziesler, J. Kim , **V. S. Sathe** and M. C. Papaefthymiou, "A 225 MHz resonant clocked ASIC," in *Int. Symposium Low-Power Electronic Design(ISLPED)*, pp. 48–53, Seoul, South Korea, Aug. 2003.

C. Patents

1. **V. S. Sathe** and S. Naffziger, "Method to safely transition from resonant clocked mode to conventional clocked mode" submitted to US Patent and Trademark Office, Jul. 2012.
2. **V. S. Sathe**, S. Naffziger, "Method of dynamically optimizing the impedance of a resonant clock switch", submitted to US Patent and Trademark Office, Jul. 2012.
3. **V. S. Sathe**, S. Arekapudi, C. Ouyang and K. Viau, "Method of safely entering and existing resonant clocking mode", submitted to US Patent and Trademark Office, Jul. 2012.
4. **V. S. Sathe** and S. Naffziger "Method for programmable clock drive in digital circuits", submitted to US Patent and Trademark Office, Jul. 2012.
5. **V. S. Sathe**, S. Naffziger and S. Arekapudi "Method to implement resonant clock driver for frequency-scalable systems", submitted to US Patent and Trademark Office, Jul. 2012.

6. **V. S. Sathe**, S. Naffziger and S. Pant, "Clock stretcher for voltage droop mitigation," submitted to US Patent and Trademark Office, Jan. 2011.
7. **V. S. Sathe** and S. Naffziger, "Oscillator device and method thereof," submitted to US Patent and Trademark Office, Dec. 2010.
8. **V. S. Sathe**, S. Naffziger, and S. Arekapudi, "Sense amplifier monotizer", submitted to US Patent and Trademark Office, Dec. 2010.
9. S. Kosonocky, S. Naffziger, and **V. S. Sathe** "Interposer including voltage regulator and method thereof," US Patent Application 2010/0072961 Sep. 23, 2008.
10. J-Y. Chueh, J. Kao, **V. S. Sathe**, and M. C. Papaefthymiou, "Clock distribution network architecture with clock skew management," US Patent 7 956 664, 3 Dec. 2007.
11. J-Y. Chueh, J. Kao, **V. S. Sathe**, and M. C. Papaefthymiou, "Clock distribution network architecture for resonant-clocked systems," US Patent 7 719 316, 3 Dec. 2007.
12. J-Y Chueh, J. Kao, **V. S. Sathe**, and M. C. Papaefthymiou, "Clock distribution network architecture with resonant clock gating," US Patent 7719 317, 3 Dec. 2007 .
13. M. C. Papaefthymiou, **V. S. Sathe**, and C. H. Ziesler, "Energy recovery boost logic," US Patent 7 355 454, 15 Jun 2005.

DESIGN AND TEST EXPERIENCE - TEST AND PRODUCTION CHIPS

1. 2012 - Emperor Test-chip. Switching regulator design. (28nm)
2. 2011 - Steamroller Volume x86-64 commercial processor. Resonant clock lead. (28nm)
3. 2010 - Piledriver Volume x86-64 commercial processor. Resonant clock lead. (32nm)
4. 2009 - Bulldozer Volume x86-64 commercial processor. Clock network and power-gating design. (32nm)
5. 2008 - Southpaw Test-chip. Sub-picosecond delay measurement, programmable critical path sensitivity selection. Switched capacitor voltage converter. (32nm)
6. 2007 - Aqua Test-chip with linear regulator for microprocessor loads. (32nm)
7. 2006 - RF1 Test-chip with Integrated single-phase resonant-clocked ASIC. (0.13μm)
8. 2006 - RF2 Test-chip with Integrated resonant-clocked ASIC with distributed clock generation. (0.13μm)
9. 2005 - Test-chip. GHz Class Charge Recovery Logic. (0.13μm)
10. 2003 - Test-chip. Resonant Clocked Wavelet Transform Design. (0.25μm)

INVITED PRESENTATIONS

- "Resonant Clock Design for a Power-efficient High-volume x86–64 Microprocessor", IEEE Solid-State Circuits Society (Denver Chapter), May 2012.

PROFESSIONAL ACTIVITIES

A. Conference Positions

- Co-chair, technical program sub-committee, IEEE Custom Integrated Circuits Conference (CICC), 2012
- Co-chair, technical program sub-committee, IEEE Custom Integrated Circuits Conference (CICC), 2013
- Chair, technical program sub-committee, IEEE Custom Integrated Circuits Conference (CICC), 2014

B. Refereeing and Reviewing

- IEEE Journal of Solid-State Circuits (JSSC).
- IEEE Custom Integrated Circuits Conference (CICC).
- IEEE International Conference on VLSI Design.
- IEEE International Symposium on Low Power Electronics and Design (ISLPED).

- IEEE International Symposium on Quality Electronic Design (ISQED)

C. Conference Organization

- Member, technical program committee, IEEE Custom Integrated Circuits Conference. (CICC) , 2012-present
- Member, technical program committee, IEEE International Conference on VLSI Design, 2012
- Member, technical program committee, IEEE ISQED, 2014

D. Professional Societies

- Chapter Officer, Institute of Electrical and Electronics Engineers Solid-State Circuits Society. (Denver Section, 2008 – 2010)
- Member of the Institute of Electrical and Electronics Engineers. (IEEE)

AWARDS AND SCHOLARSHIPS

- AMD VP Spotlight Award – Awarded for technical achievement in the successful first-ever deployment of resonant-clocking in volume microprocessors. (2010)
- IEEE Denver Section – "Chapter of the Year". (2009)
- University of Michigan EECS Department – Selected as the best dissertation in EECS for the year and nominated for the Rackham Graduate School Distinguished Dissertation. (2007)
- University of Michigan – Fellowship. (2001)